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EXAMINER

TABONE JR, JOHN J

ART UNIT

PAPER NUMBER

2138

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

|                              |  |  |  |
|------------------------------|--|--|--|
| <b>Office Action Summary</b> | <b>Application No.</b><br>09/933,468   | <b>Applicant(s)</b><br>MACLELLAN, CHRISTOPHER S. |  |
|                              | <b>Examiner</b><br>John J. Tabone, Jr. | <b>Art Unit</b><br>2138                          |  |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 12 June 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 June 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. Claim 1-24 remain pending in the current application. Claims 1, 6, 9, 10, 13, 18 and 21 have been amended.
2. In response to Applicant's amendment filed 06/12/2006, the Examiner has withdrawn the objection to the Drawings and 35 U.S.C. 112, second paragraph rejections.

### ***Response to Arguments***

3. Applicant's arguments filed 06/12/2006 have been fully considered but they are not persuasive.

Applicant submitted an Affidavit under 37 C.F.R. 1.131 in order to establish the invention recited in claims 1-24 was conceived and reduced to practice as early as September 14, 2001. The Examiner asserts that there is no establishment of how the code in exhibit A is corresponding to the claimed limitation since the claimed invention is hardware and a method using the hardware per say. As such, the Applicant needs to show that (a) the code corresponds to the claims and (b) that it worked for its intended purpose (testing etc.) in order to establish reduction to practice.

It is the Examiner's conclusion that independent claims 1, 10, 13 and 22 are not patentably distinct or non-obvious over the prior arts of record namely, Evans (US-6966017). Therefore, the rejection is maintained. Based on their dependency on

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independent claims 1, 10, 13 and 22, claims 2-9, 11-12, 14-21 and 23-24, respectively, stand rejected.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 2, 6-8, 13, 14, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Evans (US-6966017), hereinafter Evans.

#### **Claims 1, 2, 13 and 14:**

Evans teaches a BIST controller 13 (**a first logic section, BIST logic** as per claims 2 and 14), which initiates the self-test procedure that supplies test data from data generator 17 (**one or more test related signals...during test mode, test input signals** as per claims 2 and 14) for the associated instruction cache block 11 (SUT). Evans also teaches OR gate 21 (**a third logic section**) will apply a control signal to switch the selector/multiplexers 23, 25, 27 (also part of **a third logic section that selectively couples the first logic section or the second logic section to the SUT**) and 29 from their normal settings to their test settings in response either to a signal from the BIST controller 13 (**the other of the two control signals...from the first logic**

**section) or a tst\_test\_mode signal input from the JTAG controller (one of the two control signals...from a source that is external...).** In its normal setting, the multiplexers 23, 25, 27 supplies normal control, instruction data, and address information from the other elements on the chip (**second logic section that transmits signals during normal mode**). Normally, these instructions come from the processor on the chip. (Col. 6, l. 54 to col. 8, l. 17).

Claims 6 and 18:

Evans teaches the respective assertion state of the one of the two control signals (a tst\_test\_mode signal input from the JTAG controller). (Col. 7, ll. 4-8).

Claims 7 and 19:

Evans substantially teaches all the claimed limitations in that The BIST engine comprises the self-test hardware multiplexed at the front end of the cache to supply all stimuli and the MISR 19 multiplexed at the back end to computes the signature. The MISR 19 receives and processes the `miss` output as well as the instruction data output (`instout`) from the cache memory block 11. The MISR 19 calculates a test signature based on the shifting of these two outputs from the cache and the attendant feedback of values from the shifted data, as the BIST controller cycles through the test procedure. (Col. 11, ll. 13-17, col. 9, ll. 4-12).

Claims 8 and 20:

Evans teaches OR gate 21 (**a third logic section**) will apply a control signal to switch the selector/multiplexers 23, 25, 27 (also part of **a third logic section that selectively couples the first logic section or the second logic section to the SUT**)

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and 29 from their normal settings to their test settings in response either to a signal from the BIST controller 13 or a tst test mode signal input from the JTAG controller (**if both control signals are asserted...**). In its normal setting, the multiplexers 23, 25, 27 supplies normal control, instruction data, and address information from the other elements on the chip (**if at least one of the control signals is unasserted...**). (Col. 7, ll. 4-10, col. 8, l. 4-24).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 10, 11, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evans (US-6966017), hereinafter Evans.

#### Claims 10 and 22:

Evans teaches a BIST controller 13 (**a first logic section, BIST logic** as per claims 2 and 14), which initiates the self-test procedure that supplies test data from data generator 17 (**one or more test related signals...during test mode, test input signals** as per claims 2 and 14) for the associated instruction cache block 11 (SUT). Evans also teaches OR gate 21 (**a third logic section**) will apply a control signal to switch the selector/multiplexers 23, 25, 27 (also part of **a third logic section that selectively couples the first logic section or the second logic section to the SUT**)

and 29 from their normal settings to their test settings in response either to a signal from the BIST controller 13 (**the other of the two control signals...from the first logic section**) or a tst\_test\_mode signal input from the JTAG controller (**one of the two control signals...from a source that is external...**). In its normal setting, the multiplexers 23, 25, 27 supplies normal control, instruction data, and address information from the other elements on the chip (**second logic section that transmits signals during normal mode**). Normally, these instructions come from the processor on the chip. (Col. 6, l. 54 to col. 8, l. 17).

Evans does not explicitly teach "**a plurality of second logic sections**" and "**a plurality of third logic sections**". However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to duplicate Evans' second logic section (other elements on the chip, i.e. processor on the chip) and third logic section (OR gate 21, selector/multiplexers 23, 25, 27). Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made because it is well known the art that a system such as Evans' has multiple cache memories which all have to be tested. The artisan would be motivated to do so since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8 (7<sup>th</sup> Cir. 1977).

Claims 11 and 23:

Evans teaches the testing system is comprised in an ASIC (Fig. 1 is part of an IC, col. 4, ll. 37-38). Evans suggests the source (i.e. the another control signal of claims 10 and 22) is external to the ASIC in that the OR gate 21 receives the tst\_bist\_mode

signal (**the another control signal**), from a JTAG controller on the IC chip (**a source external ...**), however, the illustrated circuitry will provide the inventive self-test for the cache in response to the reset and run signals, regardless of the source thereof external to the ASIC). (Col. 6, l. 62 to col. 7, l. 3).

6. Claims 3-5, 12, 15-17 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evans (US-6966017), hereinafter Evans, in view of Miner (US-6370661), hereinafter Miner.

Claims 3 and 15:

Evans does not explicitly teach that "the first logic section (BIST engine) provides an indication signal to the second logic section (other elements on the chip normally a processor) for indicating when the first logic section (BIST engine) is attempting to test the SUT (cache memory)". Miner teaches in an analogous art a configurable (programmable) BIST architecture that dynamically interacts with a test controller (I/O controller). Miner also teaches the test sequences within the test management logic 570 (BIST) are configurable. More specifically, the test sequences that are designed into the test management logic 570 (BIST) are non-specific, that is, they can be configured with test parameters, provided by the test controller 580, to execute accesses to any memory 510, within any address range, to read or write any data pattern. The test management logic 570 accepts test parameters in a configuration register 572 that are transferred from the test controller 580 (I/O controller) over the test control bus 575 and the results of a test sequence can be accessed by the test controller 580 (I/O controller)



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in result register 573. In one embodiment, the configuration register 572 and the result register 573 are JTAG registers. Miner further teaches test execution logic 560 (also part of BIST) directly drives address, data, and control signals on the local bus 532 to directly access each of the memories 510. Miner also discloses prior to executing a test sequence, the test execution logic 560 sends a test signal 565 to the bus unit 530 (**an indication signal to the second logic section**) to preclude contention on the local bus 532, thus effectively disabling the bus unit 530 during testing. (Col. 9, l. 51 to col. 11, l. 55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Evans' BIST engine (BIST controller 13, data generator 17 and address generator 15) with Miner's configurable (programmable) BIST architecture. The artisan would be motivated to do so because it would enable Evans' BIST engine sends a test signal 565 (**an indication signal**) to the bus unit 530 (**the second logic section**, i.e. Evans' other elements on the chip) to preclude contention on the local bus 532, thus effectively disabling the bus unit 530 during testing (**for indicating when the first logic section (BIST engine) is attempting to test the SUT (cache memory)**). (see Miner, col. 11, ll. 47-55).

Claims 4 and 16:

Evans in view of Miner discloses the second logic provides to the I/O controller (test controller 580) an indication that the testing of the SUT (cache memory) is occurring (a test signal 565). Evans in view of Miner also discloses the I/O controller (test controller 580) is external to the first logic section (BIST engine), the second logic

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section (other elements on the chip, bus unit 530), the third logic section (OR gate 21, and selector/multiplexers 23, 25, 27), and the SUT. (Col. 9, l. 51 to col. 11, l. 55).

Claims 5 and 17:

Evans in view of Miner discloses prior to executing a test sequence, the test execution logic 560 sends a test signal 565 (an indication signal) to the bus unit 530 (the second logic section) to preclude contention on the local bus 532, thus effectively disabling the bus unit during testing 530 (**data transfer to be invalidated**). (Col. 11, ll. 21-24).

Claims 12 and 24:

The coupling of the first logic section to each of the third and second logic sections is rejected as per claims 10 and 22 above. Evans does not explicitly teach that the BIST engine is "programmable". However, Evans does teach that the BIST engine includes a BIST controller 13 and a data generator 17, which creates different background patterns in response from the BIST controller 13. Miner teaches in an analogous art a configurable (programmable) BIST architecture that dynamically interacts with a test controller. Miner also teaches the test sequences within the test management logic 570 (BIST) are configurable. More specifically, the test sequences that are designed into the test management logic 570 (BIST) are non-specific, that is, they can be configured with test parameters, provided by the test controller 580, to execute accesses to any memory 510, within any address range, to read or write any data pattern. The test management logic 570 accepts test parameters in a configuration register 572 that are transferred from the test controller 580 over the test control bus

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575 and results of a test sequence can be accessed by the test controller 580 in a result register 573. In one embodiment, the configuration register 572 and the result register 573 are JTAG registers. Miner further teaches test execution logic 560 (also part of BIST) directly drives address, data, and control signals on the local bus 532 to directly access each of the memories 510. (Col. 9, l. 51 to col. 11, l. 55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Evans' BIST engine (BIST controller 13, data generator 17 and address generator 15) with Miner's configurable (programmable) BIST architecture. The artisan would be motivated to do so because it would enable Evans to allow an operator full flexibility through the test controller 580 to configure any specific sequence of memory accesses to a memory 510. (see Miner, col. 11, ll. 47-55).

7. Claims 9 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evans (US-6966017), hereinafter Evans, in view of Walker (US-6539503), hereinafter Walker.

Claims 9 and 21:

Evans teaches the SUT is a memory (instruction or data cache block 11). (Col. 4, 37-41, col. 18, ll. 8-14). Evans does not explicitly teach "the second section transmits an erroneous value to be stored in the memory that may be detected during testing".

Walker teaches in an analogous art error injector 630 injects an error into a codeword variable (**an erroneous value to be stored in the memory**) that is prompted by a triggering condition or event. (Col. 6, ll. 24-42). It would have been obvious to one of

ordinary skill in the art at the time the invention was made to modify Evans' second logic section (other elements on the chip, a processor on the chip) to include Walker's error injector 630. The artisan would be motivated to do so because it would enable Evans the flexibility to inject errors, i.e. erroneous values, into a memory location in the cache memory for later detection by the Evans' BIST engine.

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

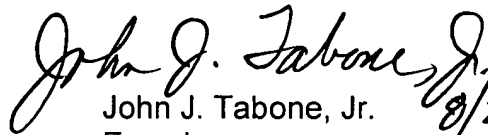
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

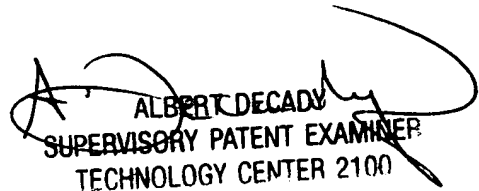
Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
John J. Tabone, Jr.  
Examiner  
Art Unit 2138  
8/29/06

  
ALBERT DECADY  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100